In the Claims:

1. (currently amended) An arrangement for suppressing digital-to-analog converter (DAC) error arising from mismatched elements contained in a DAC that is part of a modulator that provides a digital output, the arrangement comprising:

a modulator having a DAC as a part thereof and having a digital output;

~~a digital output from said modulator, said modulator having a DAC as a part thereof;~~ and

circuitry providing a shifting arrangement configured to controllably shift a digital word derived from the digital output to cause the ~~said DAC~~ error distribution from said DAC to constitute a low pass profile suppressing DAC error at higher frequencies around half a sampling frequency.

2. (previously presented) The arrangement of Claim 1, wherein:

the shifting arrangement controllably shifts the digital word using only a single pointer per clock cycle.

3. (previously presented) An arrangement for suppressing digital-to-analog converter (DAC) error arising from mismatched elements contained in a DAC that is part of a modulator that provides a digital output, the arrangement comprising:

a shifting arrangement configured to controllably shift a digital word derived from the digital output to cause a DAC error distribution to constitute a low pass profile suppressing DAC error at higher frequencies around half a sampling frequency;

wherein the shifting arrangement controllably shifts the digital word using only a single pointer per clock cycle; and

a low pass averaging (LPA) index decoder that is configured to control the shifting arrangement to shift the digital word in a manner that causes the DAC error distribution to constitute the low pass profile.

4. (previously presented) The arrangement of Claim 3, wherein the LPA index decoder is configured to provide an output according to an expression

$$LPA(j) = LPA(j-1) + \tfrac{1+(-1)^j}{2} n_Q + \tfrac{1-(-1)^j}{2}(2^N - n_Q)$$

wherein:

LPA(j) denotes a current pointer value output by the LPA index decoder;

LPA(j-1) denotes a previous pointer value output by the LPA index decoder;

N is a total number of bits in the digital word;

n_Q is a number of logic “1” bits in the digital word; and

j is a clock signal index number.

5. (previously presented) The arrangement of Claim 3, wherein the LPA index decoder includes:

a first plurality of logic gates, each having a first input and a second input, and a first output that is turned on only when a logic 0 is input to the first input and a logic 1 is input to the second input, wherein the first outputs from the first plurality of logic gates collectively control the shifting arrangement at odd numbered clock cycles; and

a second plurality of logic gates, each having a first input and a second input, and a second output that is turned on only when a logic 1 is input to the first input and a logic 0 is input to the second input, wherein the second outputs from the second plurality of logic gates collectively control the shifting arrangement at even numbered clock cycles.

6. (previously presented) The arrangement of Claim 3, further comprising a swapper, configured to receive the digital output and to provide to the shifting arrangement, on alternating clock cycles, respectively:

i) the digital output; and

ii) a swapped output containing bits of the digital output in reverse order.

7. (previously presented) The arrangement of Claim 3, wherein:

the digital output, the digital word input to the shifting arrangement and an output of the shifting arrangement, are all thermometer codes.

8. (previously presented) The arrangement of Claim 1, further comprising:

a low pass averaging (LPA) index decoder that is configured to control the shifting arrangement to shift the digital word in a manner that causes the DAC error distribution to constitute the low pass profile.

9. (previously presented) The arrangement of Claim 8, wherein the LPA index decoder is configured to provide an output according to an expression:

$$LPA(j) = LPA(j-1) + \tfrac{1+(-1)^j}{2} n_Q + \tfrac{1-(-1)^j}{2} (2^N - n_Q)$$

wherein:

LPA(j) denotes a current pointer value output by the LPA index decoder;

LPA(j-1) denotes a previous pointer value output by the LPA index decoder;

N is a total number of bits in the digital word;

n_Q is a number of logic "1" bits in the digital word; and

j is a clock signal index number.

10. (previously presented) The arrangement of Claim 8, wherein the LPA index decoder includes:

a first plurality of logic gates, each having a first input and a second input, and a first output that is turned on only when a logic 0 is input to the first input and a logic 1 is input to the second input, wherein the first outputs from the first plurality of logic gates collectively control the shifting arrangement at odd numbered clock cycles; and

a second plurality of logic gates, each having a first input and a second input, and a second output that is turned on only when a logic 1 is input to the first input and a logic 0 is input to the second input, wherein the second outputs from the second plurality of logic gates collectively control the shifting arrangement at even numbered clock cycles.

11. (previously presented) The arrangement of Claim 8, further comprising a swapper, configured to receive the digital output and to provide to the shifting arrangement, on alternating clock cycles, respectively:

i) the digital output; and

ii) a swapped output containing bits of the digital output in reverse order.

12. (previously presented) The arrangement of Claim 8, wherein:

the digital output, the digital word input to the shifting arrangement and an output of the shifting arrangement, are all thermometer codes.

13-20 (canceled)

21. (previously presented) A method for suppressing digital-to-analog converter (DAC) error arising from mismatched elements contained in a DAC that is part of a modulator that provides a digital output, the method comprising the steps of:

providing said modulator having a DAC and a digital output; and

controllably shifting a digital word derived from the digital output to cause a DAC error distribution to constitute a low pass profile suppressing DAC error at higher frequencies around half a sampling frequency.

22. (previously presented) The method of Claim 21, wherein the shifting step includes:

shifting the digital word using only a single pointer per clock cycle.

23. (previously presented) A method for suppressing digital-to-analog converter (DAC) error arising from mismatched elements contained in a DAC that is part of a modulator that provides a digital output, the method comprising:

controllably shifting a digital word derived from the digital output to cause a DAC error distribution to constitute a low pass profile suppressing DAC error at higher frequencies around half a sampling frequency;

wherein the shifting step includes shifting the digital word using only a single pointer per clock cycle and

using a low pass averaging (LPA) index decoder to cause the digital word to be shifted in a manner that causes the DAC error distribution to constitute the low pass profile.